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Published in:
Microelectronics Reliability

DOI (link to publication from Publisher):
10.1016/j.microrel.2017.06.093

Publication date:
2017

Document Version
Accepted author manuscript, peer reviewed version

A Survey of SiC Power MOSFETs Short-Circuit Robustness and Failure Mode Analysis

L. Ceccarelli, P. D. Reigosa, F. Iannuzzo, F. Blaabjerg
Center of Reliable Power Electronics, Department of Energy Technology
Aalborg University, Pontoppidanstræde 101, 9220 Aalborg, Denmark
lce@et.aau.dk, asb@et.aau.dk, fia@et.aau.dk, fbl@et.aau.dk

***Abstract* - The aim of this paper is to provide an extensive overview about the state-of-art commercially available SiC power MOSFET, focusing on their short-circuit ruggedness. A detailed literature investigation has been carried out, in order to collect and understand the latest research contribution within this topic and create a survey of the present scenario of SiC MOSFETs reliability evaluation and failure mode analysis, pointing out the evolution and improvements as well as the future challenges in this promising device technology.**

***Keywords* – SiC MOSFETs; short-circuit; failure mechanisms; short-circuit ruggedness.**

1. INTRODUCTION

Silicon carbide (SiC) power electronic devices represent an attractive alternative to traditional silicon-based power devices in many power electronics applications. Wide bandgap (WBG) semiconductor materials offer a number of noteworthy physical properties for the manufacturing of power electronic switches, such as increased power density, high voltage withstanding capability, fast switching characteristics, high temperature operation with increased efficiency [1], [2]. The latest improvements in the technological processes used in the production of SiC devices have made them rather competitive with silicon (Si) IGBTs [3]. Though SiC MOSFETs are becoming more popular, the scarce reliability evaluation and high cost, especially for power multichip modules, still hinders their diffusion into the

TABLE I – SIC DEVICES TESTED IN LITERATURE

	Manufacturer	Reference	Vds [kV]	Id [A]	Area [cm^2]
Discrete Components (TO-247)					
D1	CREE	[5,11,12]	1.2	42	0.108
D2	CREE	[9-13]	1.2	32	0.082
D3	CREE	[5,8,9]	1.2	20	0.068
D4	ROHM	[5,12]	1.2	40	0.104
Power Modules					
M1	ROHM	[6,7]	1.2	180	0.160
M2	ROHM	[6]	1.2	120	0.088
M3	Mitsubishi	[6]	1.2	400	0.375
M4	CREE	[7]	1.2	300	0.135

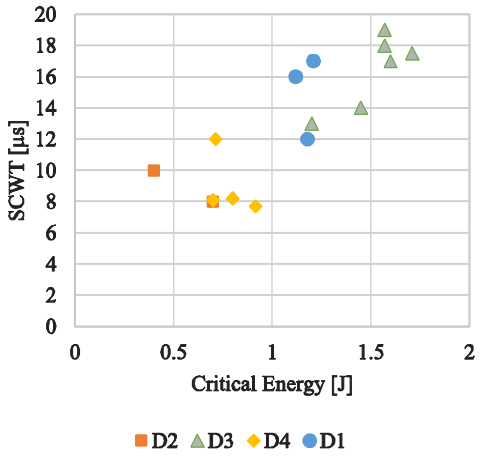

Fig. 1. Sort-circuit withstanding time (SCWT) vs. critical dissipated energy for different 1.2 kV discrete devices tested with 600 V DC-bus voltage at room temperature. Table I indicates the DUTs.

field of high-power applications, where Si IGBTs are still the first choice for the design and use in power converters. Device and package reliability as well as safe-operating area (SOA) are, in fact, considerably far below the Si technology ones [4]. A significant amount of literature has lately focused on the short-circuit (SC) robustness of SiC MOSFETs, mostly for 1.2 kV discrete devices in TO-247 package and recently also for power modules. The testing activity proves that the state-of-the-art SiC devices still present weaker short-circuit capabilities than the Si IGBT ones, and devices often fail much earlier than within 10 µs, which is the standard requirement for power electronic devices in industry. So far, several interpretations of the internal physical mechanisms responsible for the device's failure have been proposed. Furthermore, a number of electro-thermal models have been used to describe the

TABLE II – SIC MODULES SC CAPABILITY

	Manufacturer	Vdc [V]	SCWT [µs]	Energy [J]
M1	ROHM	800	5.9	5.42
M2	ROHM	800	6.2	7.29
M3	Mitsubishi	800	5.0	4.29
M4	CREE	600	3.2	6.90

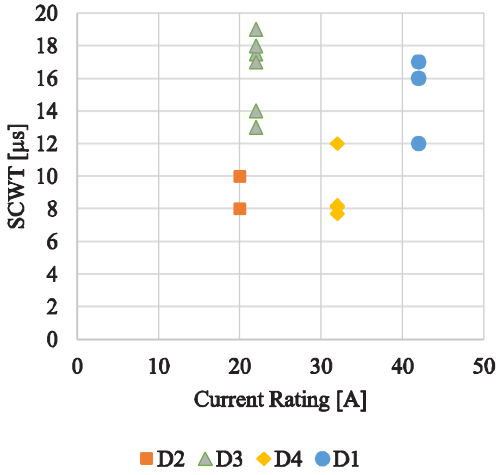

Fig. 2. Short-circuit withstanding time (SCWT) vs. current rating 1.2 kV discrete devices tested with 600 V DC-bus voltage at room temperature.

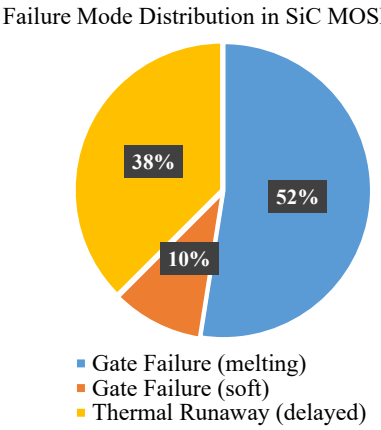

Fig. 3. Failure mode statistical distribution reported in literature for tests operated at 600V DC-bus voltage on 1.2 kV SiC devices.

semiconductor phenomena occurring during SC. Nevertheless, the results are rather scattered and sometimes disagreeing.

2. SHORT-CIRCUIT CAPABILITY

Table I reports a list of the components, which have been tested under SC in the literature [5]–[13]. A chart of the SC withstanding time (SCWT) and the relative critical energy, i.e. the amount of energy absorbed by the device before failure, is reported in Fig. 1 for the experiments carried out on discrete devices with 600 V DC-bus voltage. Table II shows the SC capability for multi-chip power modules [6]. Some of the discrete devices and none of the modules can withstand more than 10 µs SC time. Fig. 2 shows SCWT of the discrete components vs. their current rating. It is worth to notice that there is no significant correlation between SCWT and current rating. It can be assumed that for the same testing conditions, the different manufacturing process and cell structure of each device type determines the SC performances. Other studies [5], [12] have proven that there is no significant influence of the gate resistance in the SC performance, while the case temperature and DC bus voltage heavily affect the SCWT and critical energy. Moreover, the failure mode distribution for 1.2 kV devices tested at 600 V is

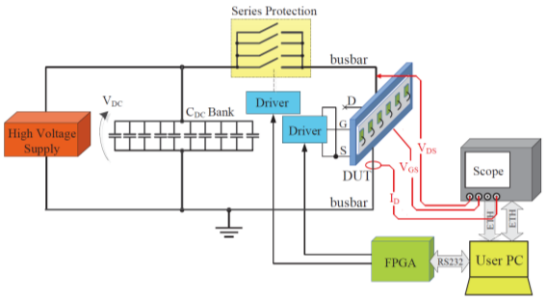

Fig. 4. Principle schematic of Non-Destructive Test setup used for SC tests [7].

reported in the chart in Fig. 3. Each of the failure modes, and the physical mechanisms behind it, is examined in detail in the next section.

3. Failure Mode Analysis

The most common failure modes according to the present literature are described in the following subsections. In addition, experimental waveforms are provided for each kind of failure, for both discrete devices and power modules. The SC waveforms have been obtained by means of a Non-Destructive Test (NDT) facility available at Aalborg University, Denmark, and presented in [7]. A schematic of the setup is depicted in Fig. 4.

3.1 Gate Oxide Breakdown

The failure mode involving the breakdown of the gate oxide is by far the most common reported in the literature (62% of the 40 reported failures). This can be observed at high DC-bus voltage SC tests with more than 50% of the rated drain-to-source voltage. The plots in Fig. 5 and 6 show a gate breakdown failure for a discrete device (D2) and a power module (M4) at room temperature, respectively. In both cases the failure occurs during turn-off, the control over the channel is lost and the current increases abruptly. A sudden increase in the junction temperature, due to the huge heat generation, damages the oxide layer. The reliability issues of gate oxides for SiC planar devices has been discussed in [2] and [14]. Essentially, in order to keep the gate voltage threshold at reasonably low

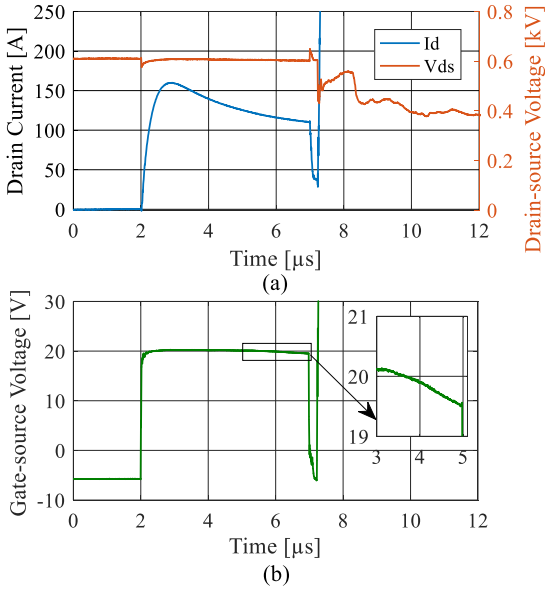

Fig. 5. Gate breakdown failure after 5 µs for a D2 device at room temperature (T_a = 25°C): drain current and drain-source voltage (a); gate voltage (b).

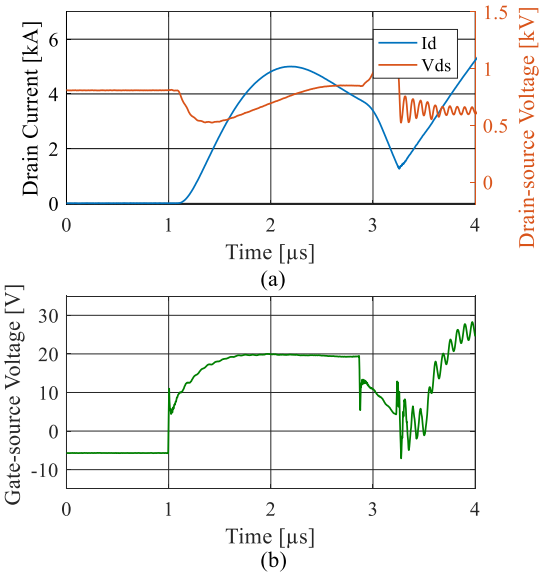

Fig. 6. Gate breakdown failure for an M4 module at room temperature (T_a = 25°C): drain current and drain-source voltage (a); gate voltage (b).

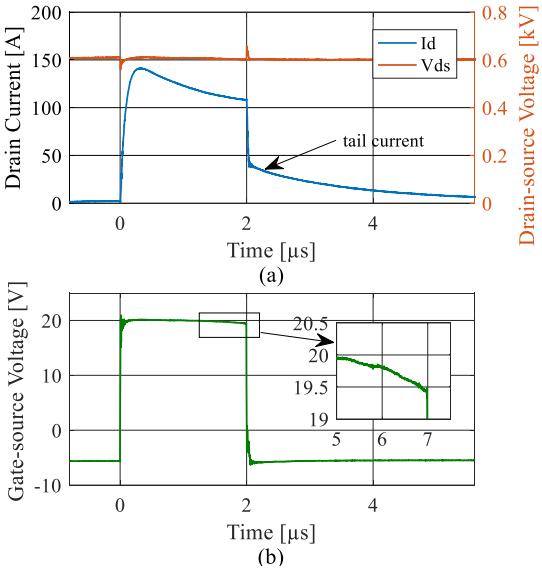

Fig. 7. Safe turn-off of D2 after 5 µs and T_a = 150°C exhibiting large tail current: drain current and drain-source voltage (a); gate voltage (b).

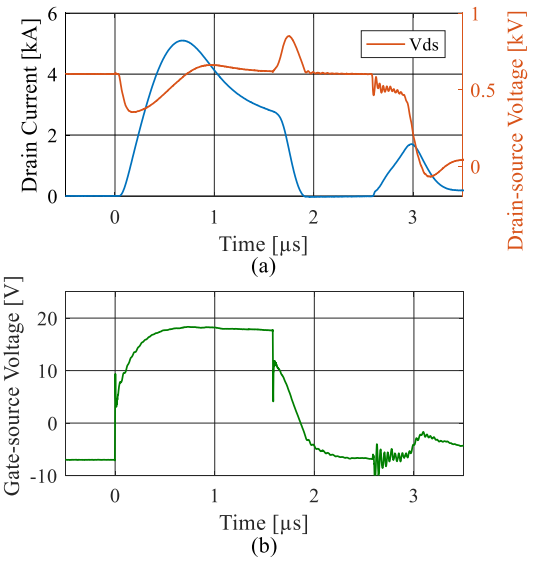

Fig. 9. Thermal runaway failure for an M4 module at room temperature (T_a = 25°C): drain current and drain-source voltage (a); gate voltage (b).

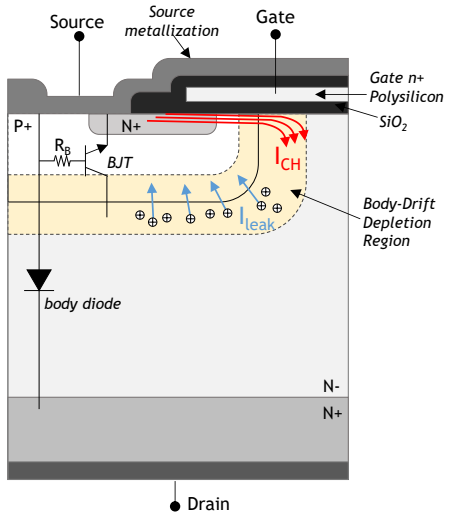

Fig. 8. SiC MOSFET cell structure cross-sectional area during thermal runaway, including body diode and parasitic BJT. I_{CH}: channel SC current; I_{leak}: drain leakage current.

values, a thinner oxide layer is used in SiC devices. This is more sensitive to higher drain voltage gradients and can result in a gate leakage current, which is further increased by a high-temperature pulse. A gate voltage drop can be observed before the failure, evidencing that the oxide is compromised and gate leakage has significantly increased. In most of the cases, the failure results in a 3-terminal short circuit due to a melting of the whole structure. The studies in [5] and [15] report instead a gate 'soft' failure, i.e. a degradation of the gate structure after repetitive SC pulses, no longer allowing control over the channel. In such cases the device cannot be turned on anymore, but it is not entirely destroyed and preserves drain-blocking capability.

3.2 Thermal Runaway Failure

The local sudden increase of temperature in the single cell can trigger physical mechanisms that lead to failure in most of the cases [16]. The high energy released in the MOSFET channel region increases temperature and, eventually, the thermal generation in the body/drift junction depletion region [17]. The drift of the generated carriers creates a drain leakage

current, which can reach considerable values and trigger a positive temperature feedback. A tail current is clearly visible in Fig. 7(a) and its peak value is higher than the rated current for the device (D2). Such a current should not be present in unipolar devices. The SiC MOSFET cell structure (visible in Fig. 8) is much thinner and narrower compared to Si devices, thanks to the SiC material properties, which in turn allows for higher power densities. Thus, the energy density is relatively higher and the junction temperature during SC can even reach 1000 K [13]. The heat dissipation is slower than the leakage current increasing rate. This behavior is the reason for a delayed failure mode (after device turn off) like the one that is observed in Fig. 9. Local defects or slight manufacturing differences can induce a weaker cell to absorb more current than the ones nearby [15], [18]. The process is irreversible and causes the formation of a *hot spot* [19] in the die with uneven current density and temperature, which leads to melting of the structure [20] with a drain-to-source shorting as a result. In power modules, this phenomenon is possibly even worsened by the unbalanced current sharing among the paralleled dies because of manufacturing mismatches. The injection of minority carriers (holes) in the p-body region can also trigger another mechanism: the turn-on of the parasitic bipolar transistor (see Fig. 3) [19]. The leakage current amplification determined by the activation of the BJT accelerates the thermal runaway failure process.

4. Modeling Activity

Modeling is essential to understand the physics behind the failure mode. Table III reports the contributions given in the latest years. In [12] a rather complete physical modeling of the drain leakage current temperature-dependent behavior is given, while in [13] a thermal network is used to simulate the temperature distribution during SC. The studies carried out in [15] and [18] are based on 2D FEM numerical approaches and focus on the thermal runaway failure mode. No simulations of the gate breakdown failure mode are available so far.

TABLE III – AVAILABLE SIC MOSFET SC MODELS

Author	Year	Model	Simulation
Wang [12]	2016	Physics	-
März [13]	2016	Physics	-
Romano [15]	2016	Numerical	TCAD
Romano [18]	2016	Numerical	TCAD

5. Perspective Technology Improvements

Fast SC protection circuits have been proposed in [9] and [21] in order to safely turn off the device before it reaches the critical energy. In [22] a p-MOSFET device is presented, having a larger SOA than n-MOSFETs. So far, no further solutions at device level have been suggested in order to enhance the SC robustness of these devices. Hence, further research should systematically address the SC ruggedness of the modules and the impact of internal layout and dies paralleling on their reliability.

6. Conclusions

The presented literature overview and the experimental characterization have allowed gathering and analyzing a significant amount of information about the state-of-art of SiC MOSFETs short circuit robustness. This goal has been achieved for both discrete devices and power modules. The main conclusions from this study are:

- The increased SiC MOSFETs power density and small chip area results in a significant reduction in SCSOA;
- The physical mechanism behind the failure mode have not yet been completely understood and thoroughly explained, especially regarding the gate failure;
- Simulations offer an understanding of the physical phenomena but they are far from giving a solid contribution to the robust and reliable design of SiC-based power converters.
- So far, very limited amount of solutions have been proposed either to protect the devices or improve their SC performance.

Thus, upcoming research efforts should be more focused on these topics, especially gate reliability, to understand and tackle the issues, which, together with their higher cost, still hinder these devices from broad adoption.

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